

This Listing of Claims will replace all prior versions or listings of claims in this application.

LISTING OF CLAIMS

1. (Currently Amended) A communication device, comprising:
a signal modulator/demodulator (modem) having a digital signal processor for effecting radio communications;

a shared memory connected to the modem; and

an application processor (AP) having a central processing unit and a ~~first~~-bus master controller for controlling via a ~~first~~-common bus a plurality of external peripherals ~~and a second bus master controller for controlling via a second common bus~~, the shared memory connected to the modem,

wherein the ~~first~~-bus master controller controls the plurality of external peripherals and the shared memory by using a packet generator issuing a packet commonly receivable by the plurality of external peripherals and the shared memory over the ~~first~~-common bus, and wherein the packet includes a module device select signal for selecting one of the plurality of external peripherals and the shared memory, and

~~wherein the packet is one of a command packet or a data packet and the first bus master controller includes a multiplexer configured to receive the command packet and the data packet and output one of the command packet or the data packet to the first common bus~~

wherein the bus master controller comprises:

a bus interface for data, address, and control signal communication with the central processing unit;

a protocol converter and protocol signal controller for receiving control signals from the central processing unit through the bus interface and managing control signal flow according to a present protocol;

an address translator for receiving the address from the central processing unit through the bus interface and translating the address depending on an application module to be accessed;

a packet generator for receiving control signals from the protocol converter and protocol signal controller and a translated address from the address translator and packetizing the control signals and the translated address in a command packet;

a receive buffer for receiving data from the central processing unit through the bus interface;

a data pack unit for arranging the received data according to a specified width of a common data structure; and

a multiplexer for receiving the command packet from the packet generator and the data packet from the data pack unit and outputting one of the command packet or the data packet to the common bus.

2. (Cancelled)
3. (Previously Presented) The device of claim 1, wherein the shared memory is an SDRAM.
4. (Previously Presented) The device of claim 1, wherein the plurality of external peripherals includes at least one of an image capture module, a display, and a flash memory.

5. (Canceled)

6. (Currently Amended) The device of claim 1, wherein the selected one of the plurality of external peripherals returns a signal to the ~~first~~-bus master controller to acknowledge receipt of the command packet.

7. (Previously Presented) The device of claim 1, wherein the command packet includes:

a read/write command directed to the shared memory shared by the modem and the AP.

8. (Currently Amended) The device of claim 7, wherein data read from the shared memory is sent to the AP via ~~the~~a second common bus with a strobe signal, and wherein the strobe signal is used for strobing the data read into a register in ~~the~~a second bus master controller.

9. (Currently Amended) The device of claim 3, wherein the SDRAM includes a plurality of data banks and an interface for interfacing ~~the~~a second bus master controller via ~~the~~ a second common bus.

10. (Previously Presented) The device of claim 3, wherein the shared memory includes a first protection circuit for receiving address data from the AP and a second protection circuit for receiving address data from the modem, each for generating a protect signal upon simultaneously receiving the same address from the modem and the AP, wherein the protect signal is generated to halt memory access by one of the modem and the AP to prevent simultaneous access of the same memory cells.

11. (Currently Amended) A communication device, comprising:

a signal modulator/demodulator (modem) having a digital signal processor for effecting radio communications;

a shared memory connected to the modem; and

an application processor (AP) having a central processing unit, a first bus master controller connected to a plurality of external peripherals via a first common bus and a second bus master controller connected to the shared memory ~~and a flash memory~~ via a second common bus,

wherein the first bus master controller is configured for controlling via the first common bus the plurality of external peripherals,

wherein the second bus master controller is configured for controlling via the second common bus the shared memory connected to the modem ~~and the flash memory~~,

wherein the first bus master controller controls the plurality of external peripherals operatively connected to the first common bus by issuing a packet~~packetized command~~ commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packet~~packetized command~~ includes a module device select signal for selecting one of the plurality of external peripherals, and

wherein the first bus master controller comprises:

a packet generator for receiving control signals and an address, and packetizing

the control signals and the address in a command packet;

a data pack unit for packing data into a data packet; and

a multiplexer for receiving the command packet from the packet generator and the data packet from the data pack unit and outputting one of the command packet or the data packet to the common bus.

12. (Canceled)

13. (Previously Presented) The device of claim 11, wherein at least one peripheral of the plurality of external peripherals is an image capture module.

14. (Cancelled)

15. (Previously Presented) The device of claim 11, wherein the selected one of the plurality of peripherals returns a signal over the first common bus to the first bus master controller in the AP to acknowledge receipt of the packetized command.

16. (Cancelled)

17. Previously Presented) The device of claim 11, wherein data read from the shared memory is transmitted via the second common bus to the second bus master controller in the AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a register in the second bus master controller.

18. (Previously Presented) The device of claim 11, wherein the shared memory is an SDRAM.

19. (Previously Presented) The device of claim 18, wherein the SDRAM includes a plurality of data banks and an interface for interfacing.

20. (Previously Presented) The device of claim 18, wherein the SDRAM includes a first protection circuit for receiving address data from the AP and a second protection circuit for receiving address data from the modem and for generating a protect signal upon simultaneously receiving the same address from the modem and the AP.

21. (Currently Amended) An application processor (AP), for use in a communication device, comprising:

a central processing unit for processing data received from a plurality of external peripherals and from a shared memory; and

a ~~first~~-bus master controller for controlling via a ~~first~~-common bus the plurality of external peripherals and the shared memory; and

~~a second bus master controller for interfacing with the shared memory via a second common bus~~; wherein the shared memory is connected to a signal modulator/demodulator (modem),

wherein the ~~first~~-bus master controller controls the plurality of peripherals and the shared memory by issuing a ~~command~~-packet commonly receivable by the plurality of external peripherals and the shared memory over the ~~first~~-common bus, and

wherein the ~~command~~ packet includes a module device select signal used for selecting one of the plurality of external peripherals and the shared memory ~~and an address specifying a start address of a data transfer~~

wherein the bus master controller comprises:

a bus interface for data, address, and control signal communication with the central processing unit;

a protocol converter and protocol signal controller for receiving control signals from the central processing unit through the bus interface and managing control signal flow according to a present protocol;

an address translator for receiving the address from the central processing unit through the bus interface and translating the address depending on an application module to be accessed;

a packet generator for receiving control signals from the protocol converter and protocol signal controller and a translated address from the address translator and packetizing the control signals and the translated address in a command packet;

a receive buffer for receiving data from the central processing unit through the bus interface;

a data pack unit for arranging the received data according to a specified width of a common data structure; and

a multiplexer for receiving the command packet from the packet generator and the data packet from the data pack unit and outputting one of the command packet or the data packet to the common bus.

22. (Cancelled)

23. (Previously Presented) The device of claim 21, wherein the shared memory is an SDRAM.

24. (Previously Presented) The device of claim 21, wherein the plurality of external peripherals additionally includes at least one of an image capture module, a display, and a flash memory.

25. (Cancelled)

26. (Currently Amended) The device of claim 21, wherein the selected one of the plurality of external peripherals returns a signal to the ~~first~~-bus master controller over the ~~first~~ common bus to acknowledge receipt of the command packet.

27. (Cancelled)

28. (Currently Amended) The device of claim 21, wherein the data read from the shared memory is sent over ~~the~~a second common bus to the AP with a strobe signal, and wherein the strobe signal is used for strobing the read data into a register of ~~the~~a second bus master controller.

29. (Currently Amended) The device of claim 23, wherein the SDRAM includes a plurality of data banks and an interface for interfacing ~~the~~a second bus master controller.

30. (Currently Amended) The device of claim 23, wherein the SDRAM includes a first protection circuit for receiving address data from the AP over the second common bus and a second protection circuit for receiving address data from the modem and for generating a protect signal upon simultaneous receipt of the same address from the AP and the modem.

31. (Currently Amended) An application processor (AP) for use in a communication device comprising:

a central processing unit for processing data received from a plurality of external peripherals over a first common bus and from a shared memory over a second common bus; and

a first bus master controller for controlling via the first common bus the plurality of external peripherals; and

a second bus master controller for interfacing via the second common bus with the shared memory that is connected to a signal modulator/demodulator (modem),

wherein the first bus master controller controls the plurality of external peripherals by issuing a packet commonly receivable by the plurality of external peripherals over the first common bus, and

wherein the packet includes a module device select signal for selecting one of the plurality of external peripherals, and

~~wherein the packet is one of a command packet or a data packet and the first bus master controller includes a multiplexer configured to receive the command packet and the data packet and output one of the command packet or the data packet to the first common bus~~

wherein the first bus master controller comprises:

a bus interface for data, address, and control signal communication with the central processing unit;

a protocol converter and protocol signal controller for receiving control signals from the central processing unit through the bus interface and managing control signal flow according to a present protocol;

an address translator for receiving the address from the central processing unit through the bus interface and translating the address depending on an application module to be accessed;

a packet generator for receiving control signals from the protocol converter and protocol signal controller and a translated address from the address translator and packetizing the control signals and the translated address in a command packet;

a receive buffer for receiving data from the central processing unit through the bus interface;

a data pack unit for arranging the received data according to a specified width of a common data structure; and

a multiplexer for receiving the command packet from the packet generator and the data packet from the data pack unit and outputting one of the command packet or the data packet to the common bus.

32. (Cancelled)

33. (Previously Presented) The device of claim 31, wherein the shared memory is an SDRAM.

34. (Previously Presented) The device of claim 31, wherein the plurality of external peripherals includes at least one of an image capture module, a display, and a flash memory.

35. (Cancelled)

36. (Previously Presented) The device of claim 31, wherein the selected one of the peripherals returns a signal over the first common bus to the first bus master controller to acknowledge receipt of the command packet.

37. (Cancelled)

38. (Previously Presented) The device of claim 31, wherein the data read from the shared memory is sent to the AP over the second common bus with a strobe signal, and wherein the strobe signal is used for strobing the data read into a register in the second bus master controller.

39. (Previously Presented) The device of claim 33, wherein the SDRAM includes a plurality of data banks and an interface for interfacing with the second bus master controller over the second common bus.

40. (Currently Amended) A method of controlling a communication device having a signal modulator/demodulator (modem) for effecting radio communications, an application processor (AP) having a central processing unit, a first-bus master controller, ~~and a second-bus master controller~~, and a shared memory, the method comprising:

controlling via a ~~first~~-common bus a plurality of external peripherals using the ~~first~~-bus master controller; and

interfacing with the modem via the shared memory and ~~a second~~ the common bus using the ~~second~~ bus master controller,

~~wherein the step of controlling the plurality of external peripherals includes sending one of a data packet or a command packet commonly receivable by the plurality of external peripherals over the first common bus, and~~

~~wherein the packets includes a module device select signal for selecting one of the plurality of external peripherals~~

wherein the step of controlling the plurality of external peripherals includes:

receiving control signals from the central processing unit and managing control signal flow according to a present protocol, by using a protocol converter and protocol signal controller;

receiving an address from the central processing unit and translating the address depending on the external peripheral to be accessed, by using an address translator;

receiving control signals from the protocol converter and protocol signal controller and a translated address from the address translator and packetizing the control signals and the translated address in a command packet, by using a packet generator;

receiving data from the central processing unit by using a receive buffer;

arranging the received data according to a specified width of a common data structure, by using a data pack unit; and

receiving the command packet from the packet generator and the data packet from the data pack unit and outputting one of the command packet or the data packet to the common bus, by using a multiplexer.

41. (Cancelled)

42. (Previously Presented) The method of claim 40, wherein the shared memory is an SDRAM.

43. (Previously Presented) The method of claim 40, wherein the step of controlling includes controlling at least one of an image capture module, a display, and a flash memory included in the plurality of external peripherals.

44. (Cancelled)

45. (Currently Amended) The method of claim 40, wherein the selected one of the plurality of external peripherals returns a signal to the ~~first~~ bus master controller over the ~~first~~ common bus to acknowledge receipt of the command packet.

46. (Cancelled)

47. (Currently Amended) The method of claim 40, wherein data read from the shared memory is transmitted over ~~the~~a second common bus to the AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a register in ~~the~~a second bus master controller.

48. (Currently Amended) The method of claim 41, further including receiving address data from the AP over ~~the~~a second common bus and from the modem at the shared memory and generating a protect signal upon simultaneously receiving the same address from the modem and the AP.

49. (Cancelled)

50. (Cancelled)

51. (New) The communication device of claim 11, wherein the first bus master controller further comprises:

a protocol converter and protocol signal controller for receiving second control signals from the central processing unit through the bus interface and managing control signal flow according to a present protocol;

an address translator for receiving a second address from the central processing unit through the bus interface and translating the second address into the address depending on an application module to be accessed; and

a receive buffer for receiving the data from the central processing unit through the bus interface.